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MCGUIREWOODS, LLP 1750 TYSONS BLVD SUITE 1800 MCLEAN, VA 22102			NGUYEN, KEVIN M	
			ART UNIT	PAPER NUMBER
			2674	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/912,523

**Applicant(s)**

KWAG, JIN-OH

**Examiner**

Kevin M. Nguyen

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3,5 and 7-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3,5 and 7-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is made in response to applicant's argument filed on May 06, 2005. Claims 4 and 6 are cancelled, claims 7-10 are amended, and claims 1-3, 5, 7-26 are currently pending in the application. Applicant's arguments, see pages 7-14 with respect to the rejections of claims 1-3, 5, 7-26 under the statutory basis for the previous rejection have been fully considered and are not persuasive. Therefore, the rejection has been maintained.
2. The objection of claims 7-10 is withdrawn.
3. The rejection of claim 14 under 35 U.S.C. 112, second paragraph, is withdrawn.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 15-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. As to claim 15, the underline below show that it is undefined in the figure and in the specification as follow:

"a data line for transmitting a first data voltage and a second data voltage," line 3;

"a second switching element connected to the second gate line and the data line..." lines 6-7;

"a second liquid crystal capacitor connected to the second switching element," line 9;

"a storage capacitor connected between the second liquid crystal capacitor..."

line 10;

"a gate driver applying the first and the second data voltages to the data line" line

12;

Base on fig. 5, assume that the gate line  $Vg(n-1)$  has first, second, third, and fourth voltages. How many voltage levels are there in the gate line  $Vg(n)$  associated with how many interval, respectively.

These limitations contain various inconsistencies and/or ambiguities so that the Examiner is unable to understand the entire limitations of claim 15.

6. As to claim 16, it is not clear what the Applicant means "the first switching element and the second switching element turn on by the second voltage and turn off by the fourth voltage," line 1-3. However, Fig. 3 shows only one switching element. There is no second switching element.

This limitation contains various inconsistencies and / or ambiguities so that the Examiner is unable to understand where is the second switching element to turn on by the second voltage and turn off by the fourth voltage.

7. As to claim 17, it is not clear what the Applicant means "the third voltage of the gate signal applied to the first gate line is higher than the fourth voltage when the first data voltage is higher than the common voltages, and the third voltage of the gate signal applied to the first gate line is lower than the fourth voltage when the first data voltage is lower than the common voltages," lines 3-6, i.e, there are totally five waveforms (a), (b), (c), (d) and (e) (see figure 5). Basically, each of waveform

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corresponds to one common voltage  $V_{com}$  (c). However, Fig. 5 shows that five waveforms (a), (b), (c), (d) and (e) corresponding to one common voltage  $V_{com}$  (c) is not corrected.

This limitation contains various inconsistencies and/or ambiguities so that the Examiner is unable to understand how five waveforms (a), (b), (c), (d) and (e) corresponding to one common voltage  $V_{com}$  (c).

8. Claims 18-24 are depended on claim 15, the reasons are set forth above.

9. As to claim 25, recited in lines 1-15 of claim 25, referring to the rejection of claim 15 above.

Recited in lines 16-19 of claim 25, it is not clear what the Applicant means "the gate signal has the first, second, and third voltage during first, second, and third interval, respectively, and the first voltage turns on the first the second switching elements the second voltage turns off the first and the second switching elements". However, Fig. 3 shows only one switching element, there is no second switching element. Furthermore, the specification describes "T1 is a reset interval, T2 is a gate-on interval, and T3 is an overshoot interval," at page 12, line 8-9.

This limitation contains various inconsistencies and/or ambiguities so that the Examiner is unable to understand how the first voltage in the reset interval T1 turns on the switching element. The second voltage in the gate-on interval T2 turns off the switching element.

Recited in lines 19-21 of claim 15, it is not clear what the Applicant means "third interval precedes the first time interval, and a polarity of the third voltage with respect to

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the second voltage is the same a polarity of the data voltage with respect to the common voltage.”

Fig. 5 and fig. 7 show the overshoot interval is after the gate-on interval. This limitation contains various inconsistencies and/or ambiguities so that the Examiner is unable to understand how third interval precedes the first time interval.

Basically, each of waveform corresponds to one common voltage Vcom or 0 volt. Examiner could not determine Vcom belonging to waveform (b) Vp or (c) Vg(n) see figure 5.

This limitation contains various inconsistencies and/or ambiguities so that the Examiner is unable to understand how a polarity of the third voltage with respect to the second voltage is the same a polarity of the data voltage with respect to the common voltage.

10. Claim 26 is depended on claim 25, the reasons are set forth above.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 1-3, 5 and 7-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al (US 6,115,018) in view of Maltese et al (US 5,841,419).

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12. As to claims 1, 5, Okumara et al teaches a liquid crystal display LCD device associated with a method, the LCD device comprising:

- a. A control signal generator 22 inputs a sync signal, inherent a clock signal, a signal line driver inputs a RGB data (see fig. 3) which defined the timing control circuit.
- b. A gate line driver 23 (a gate driver, fig. 3) applies gate signal voltage pulses (stepped-wave patterns gate voltage, fig. 5A and 5B).
- c. A signal line driver 21 (a data driver, fig. 3).
- d. The gate voltage that turned on the TFT 14 defined the gate-on (see fig. 4 and 5A).

Okumara et al teaches all of the claimed limitation of claim 1, except for "a reset interval..., and an overshoot interval..."

Maltese teaches a related a liquid crystal display LCD device associated with a method, the LCD device comprising: the second pulse is erasing the previous image (reset period), while the third pulse is the compensation pulse. The subsequent control voltages show the control window 2 associated to voltage 1. The data voltage segments employed in each control window on an expanded time scale: case 4 corresponding to control of a white pixel (maximum light transmission), and case 5, corresponding to control of black pixel (minimum light transmission) (col. 8, lines 33-43).

A last pulse has their peak amplitude of the row voltage (overshoot interval, col. 7, lines 25-27).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Okumara's the step-wave pattern gate voltage including erase pulse period and the peak amplitude period of the row voltage, in view of the teaching in the Maltese's reference because this would provide the maximum operation speed of the panel as taught by Maltese (col. 6, lines 52-55).

13. As to claims 2, 3, 11, 12, Maltese teaches extreme shades corresponding to white and to black (col. 7, lines 38).

14. As to claim 7, Okumura et al teaches gate voltages having the same polarity in K+1 field (see fig. 5A).

15. As to claim 8, Maltese teaches the last two pulses are consecutive and opposite polarities (col. 5, lines 11-12).

16. As to claim 9, Maltese teaches all pulse having the absolute value of the integral of the voltage with respect to time (col. 5, lines 13-14). Duration 12 and 12 microseconds with amplitude of 48 volts in connection with the last two levels having been employed (col. 8, lines 65-67, the voltage in the overshoot interval). Thus, the range  $\pm 3V$  to  $\pm 10V$  is in the range of  $\pm 0V$  to  $\pm 48V$  for the overshoot interval, (0 voltage is respect of the ground level voltage or common voltage).

17. As to claim 10, Maltese teaches duration 12 and 12 microseconds with amplitude of 48 volts in connection with the last two levels having been employed (col. 8, lines 65-67, the voltage in the overshoot interval). Thus, the overshoot interval is doubles.

18. As to claim 13, Maltese teaches from left to right in the figure 1, duration of 64, 112, 80, and 32 microseconds with amplitude of 23 volts (col. 8, lines 62-64). All pulse

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having the absolute value of the integral of the voltage with respect to time (col. 5, lines 13-14). Thus, the range  $\pm 3V$  to  $\pm 10V$  is in the range of  $\pm 0V$  to  $\pm 23V$  of the reset interval, (0 voltage is respect of the ground level voltage or common voltage).

### ***Response to Arguments***

19. Applicant's arguments filed May 06, 2005 have been fully considered but they are not persuasive.

20. In response to applicant's argument that claims 1 and 5 recite "a reset interval from converting a grayscale level of a first liquid crystal capacitor connected to a subsequent gate line through a first thin film transistor to a first extreme grayscale level, a gate-on interval, and an overshoot interval following the gate-on interval and having the polarity of a **data** voltage." Applicant's argument emphasizes "But the claims of the present application currently only deal with **data** voltage. Cf. also, Figure 2 (in which data voltage are not even shown) and co. 8, li. 46-47 (explicitly stating the same absence of illustration)" at page 14. Examiner is not convinced by Applicant's argument. As stated *supra* with respect to claims 1 and 5, Examiner finds that Maltese teaches Fig. 1 additionally showing the control window 2 associated to voltage 1. For what concerns the data voltage segments employed in each control window, the two following cases are shown in the inset 3 on an expanded time scale: case 4 corresponding to control of a white pixel (maximum light transmission), and case 5, corresponding to control of black pixel (minimum light transmission) (see col. 8, lines 35-43). Therefore, Maltese teaches the data voltage as claimed.

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21. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as modify, substitute and equivalent by Maltese, teaches an equivalent waveform assembly obtained by adding a single voltage function of the time to each selection voltage and data voltage (for more details see col. 7, lines 46-55). Therefore, it would have been obvious to one of ordinary skill in the art to replace/modify the waveform in Okumura with Maltese's waveform because this would provide convenient to use crosstalk compensated waveforms for the data voltages as taught by Maltese (col. 7, lines 29-30), and provide the maximum operation speed of the panel as taught by Maltese (col. 6, lines 52-55). Moreover, where the claimed differences involve substitution of interchangeable equivalents and the reason for the selection of one equivalent for another was not to solve an existent problem such substitution has been judicially determined to have been obvious. See *In re Ruff*, 118 USPQ 343 (CCPA 1958).

22. Applicant argues that "the selection signal art is non-analogous art to the data signal art, because the data voltages are typically intended to act on the liquid crystal capacitor, whereas the selection signal is typically intended to operate on a switching element such as transistor" at page 14. Examiner agrees with that, a person of ordinary

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skill in the thin film transistor liquid crystal display (TFT-LCD) or active matrix liquid crystal display (AMLCD) art to understand that the selection signal art is non-analogous art to the data signal art, because Maltese teaches at col. 8, lines 30-38 dealing with the selection voltage which is the scanning signal, is different at col. 8, lines 38-43 dealing with the data voltage which is providing the data for displaying, as modified by Okumura et al, teach Fig. 4 expressly showing when the selection voltage applied to the gate line (N-1) a switch 14-0 is turned ON, then the data voltage applied to signal line (M) via the switch 14-0 while the switch 14-0 is closed for the liquid crystal capacitor displayed. Therefore, the selection signal art is non-analogous art to the data signal art. Therefore, the rejections of claims 1-3, 5, 7-14 based on Okumura and Maltese have been maintained.

23. Applicant's argument to the rejection of independent claim 15 under 112, 2<sup>nd</sup> paragraph recitation "wherein a gate signal has first, second, third, and fourth voltages during sequentially arranged first, second, third and fourth time intervals, respectively" at page 11, lines 1-3. This argument is not persuasive because applicant notes at page 11, lines 1-3, the period to the left of T1, T1, T2, T3, and the period to the right of T3. Examiner finds that at least "the period to the left of T1" in figure 5 is infinite on the left at T1, it is not a period or an interval. Therefore, based on this reason the rejections of claim 15 under 112, 2<sup>nd</sup> paragraph have been maintained.

24. Applicant's argument to the rejection of independent claims 15 and 25 under 112, 2<sup>nd</sup> paragraph recite at least two limitations "a second switching element, and a second liquid crystal display capacitor." This argument is not persuasive because applicant

notes "one of ordinary skill in the art should understand from figure 3 the second switching element could be found. In response, examiner disagrees because one skilled in the thin film transistor liquid crystal display (TFT-LCD) art did not find the second switching element (TFT) and the second liquid crystal display in figure 2 or in the specification. The entire specification has not disclosed the second switching element (TFT) and the second liquid crystal display capacitor. Although the rejections of claims 15-26 "under 35 U.S.C. 112, 1<sup>st</sup> paragraph, as containing new subject matter" have not been made in previously office action. However, the rejections of claims 15-26 under 112, 2<sup>nd</sup> paragraph have been maintained.

25. In response to applicant's argument that dependent claim 17 only recite the limitation "the third voltage of the gate signal applied to the first gate line is higher than the fourth voltage when the first data voltage is higher than the common voltage." This argument is not persuasive because, as discussed *supra*, applicant emphasizes "the selection signal art is non-analogous art to the data signal art," one person of ordinary skill in the TFT-LCD art to understand that the scanning signal is different from the data voltage, how would the applicant make the comparison among the selection voltage, with the data voltage, and with the common voltage. Therefore, based on this reason the rejections of claim 17 under 112, 2<sup>nd</sup> paragraph have been maintained.

26. In response to applicant's argument that independent claim 25 recites the limitation "a polarity of the third voltage with respect to the second voltage is the same as a polarity of the data voltage with respect to the common voltage." This argument is not persuasive because, as discussed *supra*, applicant emphasizes "the selection signal

art is non-analogous art to the data signal art," one person of ordinary skill in the LCD art to understand that the scanning signal is different from the data voltage, how would the applicant make the comparison among the selection voltage, with the data voltage, and with the common voltage. Therefore, based on this reason the rejections of claim 25 under 112, 2<sup>nd</sup> paragraph have been maintained.

### ***Conclusion***

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 9:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603/6725. The fax phone


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number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see <http://portal.uspto.gov/external/portal/pair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Nguyen  
Patent Examiner  
Art Unit 2674

KMN  
February 1st, 2005



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